SPECIFICATION

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[METHOD FOR FABRICATING RAISED SOURCE/DRAIN OF SEMICONDUCTOR DEVICE]

Cross Reference to Related Applications

This application claims the priority benefit of Taiwan application serial no. 91114489, filed July 01, 2002.

Background of Invention

[0001] Field of Invention

[0002] The present invention relates to a method for fabricating a semiconductor device. More particularly, the present invention relates to a method for fabricating a raised source/drain of a semiconductor device.

[0003] Description of Related Art

[0004] Except a gate oxide layer and a gate structure, a metal-oxide-semiconductor (MOS) device also comprises a source/drain region in the substrate beside the gate structure. The source/drain region has a conductivity type different from that of the substrate. In the field of VLSI, MOS devices are widely used in various circuits, such as logical circuits and memory circuits, and are essential for the devices.

[0005] Refer to FIG. 1A~1C, which illustrate a process flow of fabricating a MOS device in the prior art in a cross-sectional view.

[0006] Refer to FIG. 1A, a substrate 100 is provided. Then, a thin oxide layer 102 and a polysilicon layer 104 are sequentially formed on the substrate 100.

[0007] Refer to FIG. 1B, the polysilicon layer 104 and the thin oxide layer 102 are

patterned to form a gate conductive layer 104a and a gate oxide layer 102a, respectively. An implantation is then performed to form a source/drain extension 108 in the substrate 100 beside the gate conductive layer 104a by using 104a as a mask.

[0008] Refer to FIG. 1C, a spacer 110 is formed on the sidewalls of the gate conductive layer 104a. An implantation is performed to form a source/drain 112 in the substrate 100 beside the spacer 110 with the gate conductive layer 104a and the spacer 110 as a mask.

[0009] The area of the source/drain region in a semiconductor device must be reduced as the device is miniaturized for higher integration. However, the miniaturization of the source/drain region increases the resistance, so the device current is decreased to cause overloading. The overloading problem can be solved by increasing the junction depth of the source/drain, but such a method results in the short channel effect and junction leakage. On the other hand, the source/drain can be formed with a shallow junction and a high dopant concentration, instead of a deeper junction, to prevent overloading, short channel effect and junction leakage simultaneously. However, the high-concentration strategy is usually not effective in preventing overloading because of the restriction of the solid state solubility. Furthermore, a method is provided in the prior art that decreases the spacer width and forms a shallow junction to prevent overloading and short channel effect. Unfortunately, the metal silicide layer on the source/drain with a shallow junction may cause unacceptable junction leakage.

Summary of Invention

[0010] Accordingly, this invention provides a method for fabricating a raised of a semiconductor device to lower the resistance of the source/drain.

[0011] This invention also provides a method for fabricating a raised source/drain of a semiconductor device to makes it feasible to form a source/drain with a shallow junction, so as to prevent the short channel effect and junction leakage.

[0012] A method for fabricating a raised source/drain of a semiconductor device of this invention is described as follows. A gate structure that comprises a gate oxide layer and a gate conductive layer is formed on a substrate. A low-energy implantation is used to form a source/drain with a shallow-junction in the substrate beside the gate

structure, wherein the implanting energy is, for example, 2~3KeV. Thereafter, a spacer is formed on the sidewalls of the gate structure. An elevated SiGe layer is formed on the gate structure and the source/drain with a shallow junction, wherein the SiGe layer on the source/drain serves as a raised source/drain of the device. The elevated SiGe layer is formed with rapid thermal chemical vapor deposition (RTCVD) using a reaction gas of Si_2H_6/GeH_4 mixture or SiH_2Cl_2/GeH_4 mixture. An implantation is performed to dope the elevated SiGe layer with P-type ions or N-type ions, and then a rapid thermal process (RTP) is conducted to anneal the elevated SiGe layer. A metal silicide layer is formed on the elevated SiGe layer to lower the resistance of the device.

[0013] Another method for fabricating a raised source/drain of a semiconductor device of this invention is described as follows. A gate structure that comprises a gate oxide layer, a gate conductive layer and a capping layer thereon is formed on a substrate. A low-energy implantation is used to form a source/drain with a shallow-junction in the substrate beside the gate structure, wherein the implanting energy is, for example, 2~3KeV. Thereafter, a spacer is formed on the sidewalls of the gate structure. An elevated SiGe layer is formed on the source/drain with a shallow junction, wherein the SiGe layer on the source/drain serves as a raised source/drain of the device. The elevated SiGe layer is formed with rapid thermal chemical vapor deposition (RTCVD) using a reaction gas of Si_2H_6/GeH_4 mixture or SiH_2Cl_2/GeH_4 mixture. An implantation is performed to dope the elevated SiGe layer with P-type ions or N-type ions, and then a rapid thermal process (RTP) is conducted to anneal the elevated SiGe layer. A metal silicide layer is formed on the elevated SiGe layer to lower the resistance of the device. In this method, the capping layer and the spacer may comprise the same material or different materials. If the capping layer and the spacer comprise different materials, the metal silicide layer can be formed on both the gate conductive layer and the elevated SiGe layer after the capping layer is selectively removed.

[0014] Since an elevated SiGe layer is formed on the source/drain with a shallow junction in this invention, the resistance of the source/drain can be lowered effectively. Therefore, the source/drain can be formed with a shallower junction to prevent the short channel effect and junction leakage.

[0015] Moreover, by using the method for fabricating a raised source/drain of a

semiconductor device of this invention, the reliability of junction contact of the source/drain and even the reliability of the whole device can be improved.

[0016] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0017] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0018] FIG. 1A~1C illustrate a process flow of fabricating a MOS device in the prior art in a cross-sectional view;

[0019] FIG. 2A~2F illustrate a process flow of fabricating a MOS device according to a first embodiment of this invention in a cross-sectional view; and

[0020] FIG. 3A~3G illustrate a process flow of fabricating a MOS device according to a second embodiment of this invention in a cross-sectional view.

Detailed Description

[0021] First Embodiment

[0022] Refer to FIG. 2A~2F, which illustrate a process flow of fabricating a MOS device according to the first embodiment of this invention in a cross-sectional view.

[0023] Refer to FIG. 2A, a thin oxide layer 202 and a conductive layer 204 are sequentially formed on a substrate 200, wherein the conductive layer 204 comprises, for example, polysilicon or other suitable conductive materials.

[0024]

Refer to FIG. 2B, a lithography process and an etching process are performed to pattern the conductive layer 204 and the thin oxide layer 202 into a gate conductive layer 204a and a gate oxide layer 202a, respectively, which two constitute a gate structure. A low-energy implantation is used to form a source/drain 208 with a

shallow-junction in the substrate 200 beside the gate structure, wherein the implanting energy is, for example, 2~3KeV. For a P-type MOSFET, the implanted ions are, for example, boron or BF_2^+ ions. For an N-type MOSFET, the implanted ions are, for example, phosphorous or arsenic ions.

[0025] Refer to FIG. 2C, a spacer 210 is formed on the sidewalls of the gate structure by, for example, performing low-pressure chemical vapor deposition (LPCVD) and then an anisotropic etching process. In detail, a conformal dielectric layer is formed on the substrate 200 with LPCVD and then etched back anisotropically to form the spacer 210. The spacer 210 comprises silicon nitride or silicon oxide.

[0026] Refer to FIG. 2D, an elevated SiGe layer 212 is formed on the gate conductive layer 204a and the source/drain 208 with a shallow junction to lower the resistance of the gate conductive layer 204a and the source/drain 208. The elevated SiGe layer 212 on the source/drain 208 serves as a raised source/drain of the device. The thickness of the elevated SiGe layer 212 is, for example, 200~500 Å . The method for forming the elevated SiGe layer 212 is, for example, rapid thermal chemical vapor deposition (RTCVD) that uses a reaction gas such as Si_2H_6/GeH_4 mixture gas or SiH_2Cl_2/GeH_4 mixture gas. In addition, the RTCVD process is conducted under a pressure such as 1~20 Torr and a temperature such as 500 ° C.

[0027] Refer to FIG. 2E, an ion implantation 214 is performed to dope the elevated SiGe layer 212 with P-type ions or N-type ions. A rapid thermal process (RTP) is then conducted to anneal the elevated SiGe layer 212 to create a required dopant profile.

[0028] It is noted that the implanted dopants, particularly boron, can be held in the elevated SiGe layer 212 and will not diffuse into other layers in subsequent thermal processes. Moreover, the resistance of the SiGe layer 212 is lower than that of the source/drain region 208, and the Ge concentration in the SiGe layer 212 can be adjusted to decrease the band gap of SiGe and thereby lower the resistance. Therefore, the source/drain 208 can be formed with a shallower junction to avoid the short channel effect and junction leakage. Consequently, the reliability of junction contact of the source/drain and even the reliability of the whole device can be improved.

[0029] Refer to FIG. 2F, a metal silicide layer 216 is formed on the elevated SiGe layer 212 covering the gate conductive layer 204a and the source/drain 208 to further reduce the resistance of the device. The method for forming the metal silicide layer 216 comprises, for example, forming a metal layer on the substrate 200, performing a thermal process to make the metal layer react with silicon to form a self-aligned silicide (salicide) layer, and then removing the unreacted metal layer. In this embodiment, the metal silicide layer 216 comprises, for example, cobalt silicide ($CoSi_x$) or nickel silicide ($NiSi_x$).

[0030] Second Embodiment

[0031] FIG. 3A~3F illustrate a process flow of fabricating a MOS device according to the second embodiment of this invention in a cross-sectional view.

[0032] Refer to FIG. 3A, a thin oxide layer 302, a conductive layer 304 and a capping layer 305 are sequentially formed on a substrate 300. The conductive layer 304 comprises, for example, polysilicon or other suitable conductive materials. The capping layer 305 comprises a material such as TEOS or silicon nitride.

[0033] Refer to FIG. 3B, a lithography process and an etching process are performed to pattern the capping layer 305, the conductive layer 304 and the thin oxide layer 302 into a gate structure. The gate structure consists of a patterned capping layer 305a, a gate conductive layer 304a and a gate oxide layer 302a. A low-energy implantation is used to form a source/drain 308 with a shallow-junction in the substrate 300 beside the gate structure, wherein the implanting energy is, for example, 2~3KeV. For a P-type MOSFET, the implanted ions are boron or BF_2^+ ions, for example. For an N-type MOSFET, the implanted ions are phosphorous or arsenic ions, for example.

[0034] Refer to FIG. 3C, a spacer 310 is formed on the sidewalls of the gate structure by, for example, performing low-pressure chemical vapor deposition (LPCVD) and then an anisotropic etching process. In detail, a conformal dielectric layer is formed on the substrate 300 covering the capping layer 305a with LPCVD and then etched back anisotropically to form the spacer 310. The spacer 310 comprises silicon nitride.

[0035] Refer to FIG. 3D, an elevated SiGe layer 312 is formed on the source/drain 308 with a shallow junction to lower the resistance of the source/drain 308. The thickness

of the elevated SiGe layer 312 is, for example, 200~500 Å . The method for forming the elevated SiGe layer 312 is, for example, rapid thermal chemical vapor deposition (RTCVD) that uses a reaction gas such as Si_2H_6/GeH_4 mixture gas or SiH_2Cl_2/GeH_4 mixture gas. In addition, the RTCVD process is conducted under a pressure such as 1~20 Torr and a temperature such as 500 ° C.

[0036] Refer to FIG. 3E, an ion implantation 314 is performed to dope the elevated SiGe layer 312 with P-type ions or N-type ions. A rapid thermal process is then conducted to anneal the elevated SiGe layer 312 to create a required doping profile.

[0037] It is noted that the implanted dopants, particularly boron, can be held in the elevated SiGe layer 312 and will not diffuse into other layers in subsequent thermal processes. Moreover, the resistance of the SiGe layer 312 is lower than that of the source/drain region 308, and the Ge concentration in the SiGe layer 312 can be adjusted to decrease the band gap of SiGe and thereby lower the resistance. Therefore, the source/drain 308 can be formed with a shallower junction to avoid the short channel effect and junction leakage. Consequently, the reliability of junction contact of the source/drain and even the reliability of the whole device can be improved.

[0038] Refer to FIG. 3F, a metal silicide layer 316 is formed on the elevated SiGe layer 312 covering the source/drain 308 to further reduce the resistance of the device. The method for forming the metal silicide layer 316 comprises the following steps, for example. A metal layer is formed on the substrate 300 covering the gate conductive layer 304a, a thermal process is performed to make the metal layer react with silicon to form a self-aligned metal silicide (salicide) layer, and then the unreacted metal layer is removed. In this embodiment, the metal silicide layer 316 comprises, for example, cobalt silicide ($CoSi_x$) or nickel silicide ($NiSi_x$).

[0039] Besides, if the capping layer 305a and the spacer 310 comprise different materials, the metal silicide layer 316 can be formed on both the gate conductive layer 304a and the elevated SiGe layer 312 after the capping layer 305a is selectively removed, as shown in FIG. 3G. In this case, for example, the capping layer 305a comprises TEOS and the spacer 310 comprises silicon nitride, so the capping layer 305a can be selectively removed. Consequently, the resistance of the gate conductive

layer 304a can also be reduced.

[0040] Since an elevated SiGe layer is formed on the source/drain with a shallow junction in this invention, the resistance of the source/drain can be lowered effectively. Therefore, the source/drain can be formed with a shallower junction to prevent the short channel effect and junction leakage.

[0041] Moreover, by using the method for fabricating a raised source/drain of a semiconductor device, the reliability of junction contact of the source/drain and even the reliability of the whole device can be improved.

[0042] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.